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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,292	02/12/2004	Florin A. Oprescu	LT-171	7415

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FISH & NEAVE LLP
1251 AVENUE OF THE AMERICAS
50TH FLOOR
NEW YORK, NY 10020-1105

EXAMINER	
YOUNG, BRIAN K	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,292	OPRESCU, FLORIN A.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-37 are objected to because of the following informalities: independent claims 1,10,19,28, and 29 ambiguously recite that "a customized buffer/amplifier may be placed" or "to be placed". The language should be changed to "is placed" or "placed". Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Oprescu et al (6,411,242).

It is noted that Oprescu et al (6,411,242) was previously filed by the same applicant. Oprescu et al (6,411,242) disclose (fig.5) a circuit for converting an analog input (Ein)at an input terminal to a digital output (y'n) at an output terminal, the circuit comprising: an analog chopper circuit (40) having an input coupled to the input terminal, and providing an output at a first predetermined rate; a first terminal and a second terminal, wherein a customized buffer/amplifier (14) may be placed across the first and second terminals such that the output of the analog chopper at a first predetermined rate is received at the first terminal and the output of the customized buffer/amplifier is received at the second terminal; a quantizer circuit (52) having an input coupled to the second terminal, and providing an output at a second predetermined rate; a first digital filter and first decimator (54) having an input coupled to the output of the quantizer circuit, and; a

second digital filter (56) having an input coupled to the output of the first digital filter and first decimator; and a second decimator having an input coupled to the output of the second digital filter, and providing the digital output.

One having basic electronics skills would know that a circuit is configured for the particular application of that circuit; therefore, the use of a "customized buffer/amplifier" in the circuit would be inherent. No specific details of the customization are given.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lui et al disclose a nested-chopper 100 delta-sigma modulator, as shown in FIG. 1 , a nested chopper 100 includes switches A and B controlled by two non-overlapped clocks .phi.A and .phi.B, which periods are multiple of chopper period. A latter chopper 100' (shown in FIGS. 3 and 4), is controlled by the clocks .phi.11 and .phi.12. The nested chopper 100 includes a first chopper section 104 that is coupled to input terminals. The first chopper section is controlled by the pair of non-overlapping clocks .phi.A and .phi.B. The second chopper section 102 is being coupled to the first chopper section 104. The output of the first chopper section 104 leads to an input of the second chopper section 102, and the second chopper section is controlled by the pair of chopper clocks .phi.11 and .phi.12. The pair of non-overlapping clocks is a multiple of the pair of chopper clocks, and the non-overlapping clocks are configured to continuously invert on a period..

Holloway et al disclose an invention, wherein a modulation system can be incorporated in an incremental or a delta-sigma ADC for sampling and digitizing analog signals generated at an impedance-varying input sensor in response to its stimulus. Both a

delta-sigma ADC and an incremental ADC include a delta-sigma (.DELTA..SIGMA.) modulator as the analog front end and digital post processing circuitry as the digital back end. The modulator samples the analog input signal, such as an input voltage generated by the input sensor, and generates a single bit digitized data stream having an ones density representative of the magnitude of the analog input signal. The digital post processing circuitry of a delta-sigma ADC may include filters, while the digital post processing circuitry of an incremental ADC may include counters, each for processing the ones density data stream. Each post processing circuit thereby generates a single digital value indicative of the relative frequency of occurrence of the many logical "1" values in the digitized data stream within some time interval. The single digital value is therefore an estimate of the average magnitude of the analog input signal during that time interval.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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